CLAIMS

What is claimed is:

1. A method comprising:

determining a cycle period of a first clock signal;

detecting rising and falling edges of a second clock signal during the cycle period of the first clock signal; and

designating the cycle period of the first clock signal as valid if a single rising edge of the second clock signal and a single falling edge of the second clock signal are detected during the cycle period of the first clock signal.

2. The method of claim 1, wherein the first clock signal is a reference clock signal and the second clock signal is a feedback clock signal.

3. The method of claim 1, wherein the determining the cycle period of the first clock signal further comprises detecting a rising edge of the first clock signal and detecting an immediately following rising edge of the first clock signal.

4. The method of claim 1, further comprising:

counting a number of consecutive cycle periods of the first clock signal that are designated as valid.

5. The method of claim 4, further comprising:

comparing a predetermined full count number to the number of consecutive cycle periods of the first clock signal that are designated as valid; and

asserting a lock signal when the predetermined full count number substantially equals the number of consecutive cycle periods of the first clock signal that are designated as valid.

6. The method of claim 4, further comprising:

comparing a predetermined full count number to the number of consecutive cycle periods of the first clock signal that are designated as valid; and

asserting a lock signal when the number of consecutive cycle periods of the first clock signal that are designated as valid exceeds the predetermined full count number by two.

7. The method of claim 1, wherein the designating the cycle period of the first clock signal as valid further comprises, detecting a single rising edge of a skewed second clock signal and a single falling edge of the skewed second clock signal during a subsequent cycle period of the first clock signal.

8. The method of claim 1, wherein the first clock signal is a reference clock signal and the second clock signal is a skewed feedback clock signal.

9. A circuit comprising:

a valid cycle detector that receives a first clock signal and a second clock signal and outputs a valid cycle signal, the valid cycle detector asserting the valid cycle signal when the valid cycle detector detects a single rising edge of the second clock signal and a single falling edge of the second clock signal during a cycle period of the first clock signal; and

a valid cycle counter that receives the first clock signal and the valid cycle signal and outputs a lock signal, the valid cycle counter counting a number of consecutive cycle periods of the first clock signal during which the valid cycle detector has asserted the valid cycle signal, the valid cycle counter asserting the lock signal when the number of consecutive cycle periods of the first clock signal during which the valid cycle detector has asserted the valid cycle signal exceeds a predetermined number.

10. The circuit of claim 9, wherein the valid cycle counter asserts the lock signal when the number of consecutive cycle periods of the first clock signal during which the valid cycle detector has asserted the valid cycle signal exceeds the predetermined number by two.

11. The circuit of claim 9, wherein the first clock signal is a reference clock signal and the second clock signal is a feedback clock signal.

12. The circuit of claim 9, wherein the first clock signal is a reference clock signal and the second clock signal is a skewed feedback clock signal.

13. The circuit of claim 9, wherein the cycle period of the first clock signal is defined between successive rising edges of the first clock signal.

14. The circuit of claim 9, wherein the valid cycle detector de-asserts the valid cycle signal after each cycle period of the first clock signal.

15. The circuit of claim 9, wherein the valid cycle counter is reset when the valid cycle detector does not assert the valid cycle signal during a second cycle period immediately prior to the first-mentioned cycle period of the first clock signal.

16. The circuit of claim 9, wherein the valid cycle counter further comprises a lock state machine and a cycle counter, the lock state machine receiving the valid cycle signal and outputting the lock signal, the lock state machine controlling when the cycle counter increments.

17. The circuit of claim 16, wherein the cycle counter counts up to the predetermined number.

18. The circuit of claim 9, wherein the valid cycle counter contains a single counter that is larger than two bits.

19. A circuit comprising:

a phase-locked loop circuit that receives a reference clock signal and generates a feedback clock signal; and

a lock detection circuit, the lock detection circuit counting a number of rising and falling edges of the feedback clock signal during a period of the reference clock signal, the lock detection circuit generating a valid cycle signal having a first value if exactly one rising edge and exactly one falling edge is counted and having a second value if another number of rising edges and falling edges is counted.

20. A circuit comprising:

a phase-locked loop circuit that receives a reference clock signal and generates a feedback clock signal; and

means for detecting whether the feedback clock signal is locked to the reference clock signal, wherein the means counts falling edges of the feedback clock signal.

21. A circuit comprising:

a locked loop circuit receiving a reference clock signal and generating a feedback clock signal;

means for detecting valid cycles of the reference clock signal wherein a valid cycle occurs when a single rising edge and a single falling edge of the feedback clock signal occur during a cycle period of the reference clock signal; and

means for outputting a lock signal when a number of consecutive valid cycles of the reference clock signal exceeds a predetermined number.